UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/721,959	11/27/2000	Junichi Kokudo	Q61990	3595

7590 08/24/2004	**EXAMINER**
SUGHRUE, MION, ZINN, MACPEAK & SEAS	MEW, KEVIN D

ART UNIT	PAPER NUMBER
2664	6

SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 Pennsylvania Avenue, N. W.
Washington, DC 20037-3202

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/16/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,6 and 9* is/are allowed.

6)☒ Claim(s) *1,3,7 and 8* is/are rejected.

7)☒ Claim(s) *2 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

    1.☐ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

Detailed Action

Response to Amendment

1.   Applicant's arguments filed on June 16, 2004 regarding claims 1-4 have been

fully considered and claims 1-9 are currently pending. Claims 7, 8 and 9 have been

added by the applicant.

Claim Objections

2.   Claim 1 is objected to because of the following informalities: "(1DMA)" should

read as "(TDMA)" in lines 1-2 of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3.   **Claims 1, 3, 7-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over

Kou (USP 5,303,234) in view of Abefelt et al. (USP 5,347,513).

Regarding claim 1, Kou discloses a slot assignment unit for use in a time division

multiple access (TDMA) transmitter (see central station, Fig. 1), comprising:

a first table (buffer 16 that stores ACK/NAK data, see element 16, Fig. 1);

a control data generation unit (decision circuit generating ACK/NAK data, see

lines 12-37, col. 4, and element 10, Fig. 1) for receiving assignment terms for a plurality

of time slots and slot data from an external source (data generated by slot assignment

circuit such as busy/idle status of minislots, see lines 56-67, col. 4), producing a set of

assignment control data (generating ACK/NAK data, see lines 12-37, col. 4) according to

the assignment terms and the slot data (according to the number of minislots detected by

the decision circuit and status of minislots detected by the decision circuit, see lines 14-

20, col. 4) and storing the set of assignment control data into an entry of said first table in

response to a command signal applied thereto (ACK/NAK data from the detection circuit

is stored in buffer 16 in response to a timing signal DS from the timing circuit 19, see

Fig. 1).

a sequence controller (slot counter, see element 20, Fig. 1) for analyzing a

plurality of said sets of assignment control data (slot counter for determining the address

pointer in order to locate the ACK/NAK data, see lines 38-40, col. 4), producing a

plurality of address pointers (slot counter supplies address pointers, see line 1, col. 5), and

for supplying said command signal to said control data generation unit in response to

each of said address pointers (slot counter for determining the location of the ACK/NAK

data from the detection circuit using the address pointer and using a dataslot timing signal

DS from timing circuit, see lines 38-41, col. 4).

Kou does not explicitly show a second table and storing said plurality of address

pointers in said second table in such a sequence that the address pointers can be

sequentially read out in a desired transmission sequence.

However, Abefelt discloses a slot analyzer for storing the address pointers in an

allocation memory and for examining and identifying the type of time slots arrived and

sequentially reading the address pointer until every time slots in a frame has been

examined (see lines 25-43, col. 16 and elements 155, 157, 161, Fig. 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to combine the TDMA transmitter of Kou with the slot

analyzer of Abefelt such that the TDMA transmitter of Kou will comprise a slot analyzer

to sequentially read address pointers pointed from one memory location to the next such

as the slot analyzer taught by Abefelt. The motivation to do so is to analyze the frame to

determine whether the time slot is a control time slot or a data time slot because different

dedicated memory units will be used to store different types of time slots.

Regarding claim 3, Kou discloses a time division multiple access (TDMA)

transmitter (see central station, Fig. 1) comprising:

a first table (buffer 16 that stores ACK/NAK data, see element 16, Fig. 1);

a control data generation unit (decision circuit generating ACK/NAK data, see

lines 12-37, col. 4, and element 10, Fig. 1) for receiving assignment terms for a plurality

of time slots and slot data from an external source (data generated by slot assignment

circuit such as busy/idle status of minislots, see lines 56-67, col. 4), producing a set of

assignment control data (decision circuit generates ACK/NAK data, see lines 12-37, col.

4) according to the assignment terms and the slot data (according to the number of

minislots and status of minislots detected by the decision circuit, see lines 14-20, col. 4)

and storing the set of assignment control data into an entry of said first table in response

to a command signal applied thereto (ACK/NAK data from the detection circuit is stored

in buffer 16 in response to a timing signal DS from the timing circuit 19, see Fig. 1).

a sequence controller (slot counter, see element 20, Fig. 1) for analyzing a

plurality of said sets of assignment control data (slot counter for determining the address

pointer in order to locate the ACK/NAK data, see lines 38-40, col. 4), producing a

plurality of address pointers (slot counter supplies address pointers, see line 1, col. 5), and

for supplying said command signal to said control data generation unit in response to

each of said address pointers (slot counter for determining the location of the ACK/NAK

data from the detection circuit using the address pointer and using a dataslot timing signal

DS from timing circuit, see lines 38-41, col. 4),

a data memory for storing a plurality of transmit data (Transmit Buffer for storing

user data, see element 13, Fig. 1); and

a framing unit (a framing unit is interpreted as a combination of slot counter,

MUX) for sequentially reading address pointers from said starting address of said second

table (a slot counter for reading address pointers, see element 20, Fig. 1) and reading

assignment control data from entries of said first table which are specified by the read

address pointers (reading ACK/NAK data from buffer 16 by reading the address pointers

of the slot counter, see lines 38-56, col. 4 and Fig. 1) and formulating a frame with the

read assignment control data and said plurality of transmit data from said data memory

(see lines 66-67, col. 4 and lines 1-5, col. 5).

Kou does not explicitly show a second table and storing said plurality of address

pointers in said second table in such a sequence that the address pointers can be

sequentially read out in a desired transmission sequence.

However, Abefelt discloses a slot analyzer for storing the address pointers in an

allocation memory and for examining and identifying the type of time slots arrived and

sequentially reading the address pointer until every time slots in a frame has been
examined (see lines 25-43, col. 16 and elements 155, 157, 161, Fig. 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the
time the invention was made to combine the TDMA transmitter of Kou with the slot
analyzer of Abefelt such that the TDMA transmitter of Kou will comprise a slot analyzer
to sequentially read address pointers pointed from one memory location to the next such
as the slot analyzer taught by Abefelt. The motivation to do so is to analyze the frame to
determine whether the time slot is a control time slot or a data time slot because different
dedicated memory units will be used to store different types of time slots.

Regarding claim 7, Kou discloses the slot assignment unit of claim 1, wherein the
assignment terms include one or more of:

priority levels classified according to at least one of communication services and
urgency,

types of packets (control field comprises a subfield which could be ACK or NAK
type, see lines 19-29, col. 3); and

an uplink-to-downlink ratio within a frame.

Regarding claim 8, Kou discloses the TDMA transmitter of claim 3, wherein the
assignment terms include one or more of:

priority levels classified according to at least one of communication services and
urgency,

types of packets (control field comprises a subfield which could be ACK or NAK

type, see lines 19-29, col. 3); and

an uplink-to-downlink ratio within a frame.

Allowable Subject Matter

4.   Claims 5-6, 9 are allowed.

5.   Claims 2, 4 are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject

matter:

In claims 2 and 4, the slot assignment unit of claim 1, wherein said set of

assignment control data stored in said table includes an address of a communication

terminal, a starting address point of each transmit data in said data memory, and a

count number of slots assigned to said entry.

In claim 5, a slot assignment method for a time division multiple access (TDMA)

transmitter, comprising the steps of:

    a)   receiving assignment terms for a plurality of time slots and slot data;

    b)   producing a set of assignment control data according to the assignment

            terms and the slot data;

c)   repeating steps (a) and (b) to produce a plurality of sets of assignment

control data;

d)   analyzing said plurality of sets of assignment control data;

e)   storing one of said sets of assignment control data into an entry of a first

table;

f)   storing an address pointer in a second table corresponding to said entry of

said first table; and

g)   repeating steps (d) to (f) until all of said assignment control data are stored

in the first table.

Response to Arguments

6.   Applicant's arguments with respect to claims have been considered but are moot

in view of the new ground(s) of rejection.

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure with respect to high speed timeslot assignment unit and method for

a TDMA communication system.

US Patent 6,728,254 to Stacey et al.

US Patent 6,064,649 to Johnston

US Patent 5,963,558 to Harada
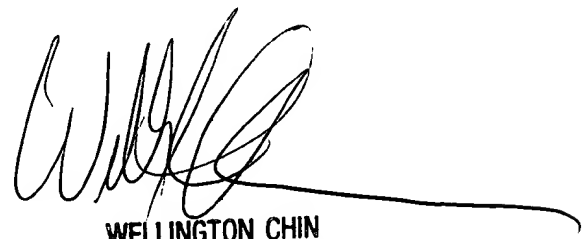
US Patent 5,862,136 to Irwin

8.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kevin Mew whose telephone number is 703-305-5300.

The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Wellington Chin can be reached on 703-305-4366. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free).

WELLINGTON CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

KDM
Art Unit 2664